Electronic Version
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Claims

[c1] 1. A method of reducing a ripple of a pulse frequency modulated (PFM) voltage regulator for converting a DC voltage source to an output voltage, comprising:
using a PFM switching signal for converting the DC voltage source to the output voltage;
detecting the output voltage; and
reducing a duty cycle of the PFM switching signal when the output voltage is lower than a predetermined target voltage, whereby:
reducing the ripple of the output voltage.

[c2] 2. The method according to claim 1, wherein:
the step of reducing the duty cycle of the PFM switching signal is implemented by prolonging a predetermined minimum OFF-time of the PFM switching signal.

[c3] 3. The method according to claim 2, wherein:
the predetermined minimum OFF-time of the PFM switching signal is prolonged in accordance with an absolute difference between the output voltage and the predetermined target voltage.

[c4] 4. The method according to claim 3, wherein:

the predetermined minimum OFF-time of the PFM switching signal is prolonged along with an increase of the absolute difference between the output voltage and the predetermined target voltage.

[c5] 5. The method according to claim 1, wherein:
the step of reducing the duty cycle of the PFM switching signal is implemented by shortening a predetermined constant ON-time of the PFM switching signal.

[c6] 6. The method according to claim 5, wherein:
the predetermined constant ON-time of the PFM switching signal is shortened in accordance with an absolute difference between the output voltage and the predetermined target voltage.

[c7] 7.Themethod according to claim 6, wherein:
the predetermined constant ON-time of the PFM switching signal is shortened along with an increase of the absolute difference between the output voltage and the predetermined target voltage.

[c8] 8.Themethod according to claim 1, wherein:
the predetermined target voltage is a DC component of the output voltage.

[c9] 9.Themethod according to claim 1, wherein:
in the step of reducing the duty cycle of the PFM switch-

ing signal, the duty cycle of the PFM switching signal is reduced in accordance with an absolute difference between the output voltage and the predetermined target voltage.

[c10] 10.Themethod according to claim 9, wherein:
the duty cycle of the PFM switching signal is reduced along with an increase of the absolute difference between the output voltage and the predetermined target voltage.

[c11] 11.Themethod according to claim 1, wherein:
the PFM voltage regulator is operated in a heavy loading condition.

[c12] 12.Themethod according to claim 1, wherein:
in the step of using the PFM switching signal for converting the DC voltage source to the output voltage, the PFM switching signal turns on a power switch transistor during an ON-time and turns off the power switch transistor during an OFF-time, in which the ON-time is shorter than or equal to a predetermined constant ON-time and the OFF-time is longer than or equal to a predetermined minimum OFF-time.

[c13] 13. A method of reducing a ripple of a pulse frequency modulated (PFM) voltage regulator including an inductive

means and a capacitive means, the inductive means being coupled to a DC voltage source and the capacitive means having a terminal coupled to the inductive means and providing an output voltage, the method comprising:

using a PFM switching signal for converting the DC voltage source to the output voltage;

detecting the output voltage; and

prolonging a period of delivering energy from the inductive means to the capacitive means when the output voltage is lower than a predetermined target voltage, whereby:

reducing the ripple of the output voltage.

[c14] 14.Themethod according to claim 13, wherein:

the period of delivering energy from the inductive means to the capacitive means is prolonged in accordance with an absolute difference between the output voltage and the predetermined target voltage.

[c15] 15.Themethod according to claim 14, wherein:

the period of delivering energy from the inductive means to the capacitive means is prolonged along with an increase of the absolute difference between the output voltage and the predetermined target voltage.

[c16] 16. The method according to claim 13, wherein:

the PFM voltage regulator is operated in a heavy loading condition, and
the predetermined target voltage is a DC component of the output voltage.

[c17] 17. A method of reducing a ripple of a pulse frequency modulated (PFM) voltage regulator including an inductive means and a capacitive means, the inductive means being coupled to a DC voltage source and the capacitive means having a terminal coupled to the inductive means and providing an output voltage, the method comprising:
using a PFM switching signal for converting the DC voltage source to the output voltage;
detecting the output voltage; and
shortening a period of storing energy in the inductive means when the output voltage is lower than a predetermined target voltage, whereby:
reducing the ripple of the output voltage.

[c18] 18.Themethod according to claim 17, wherein:
the period of storing energy in the inductive means is shortened in accordance with an absolute difference between the output voltage and the predetermined target voltage.

[c19] 19.Themethod according to claim 18, wherein:

the period of storing energy in the inductive means is shortened along with an increase of the absolute difference between the output voltage and the predetermined target voltage.

[c20] 20. The method according to claim 17, wherein:
the PFM voltage regulator is operated in a heavy loading condition, and
the predetermined target voltage is a DC component of the output voltage.